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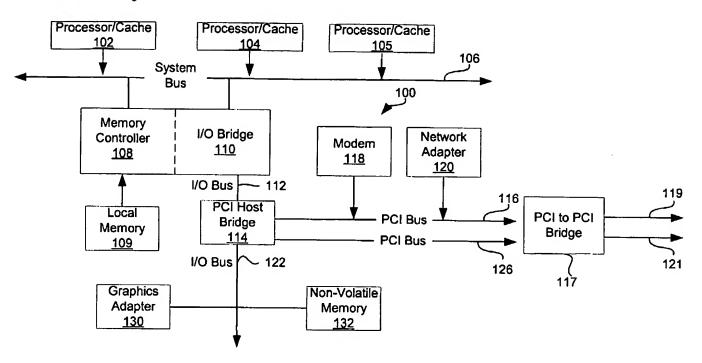
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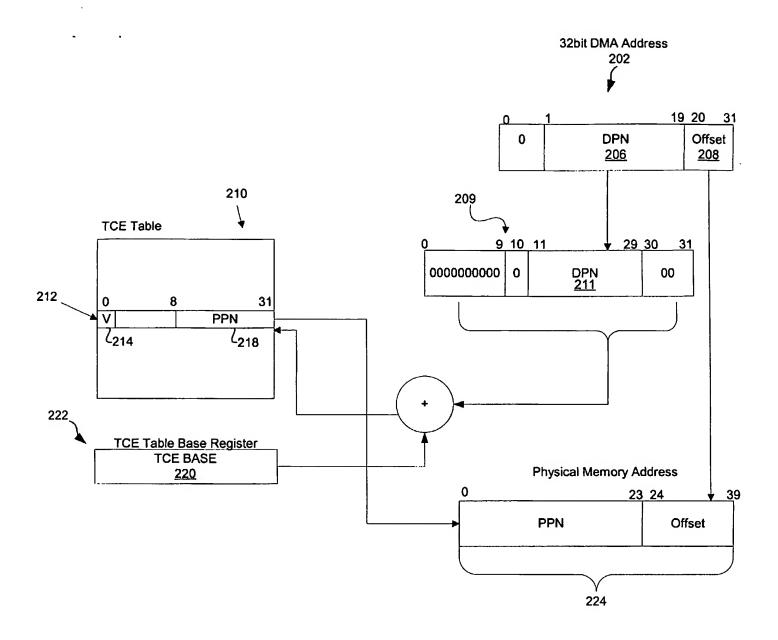
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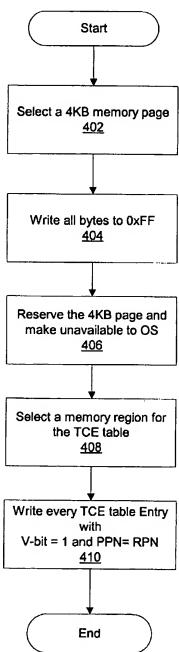


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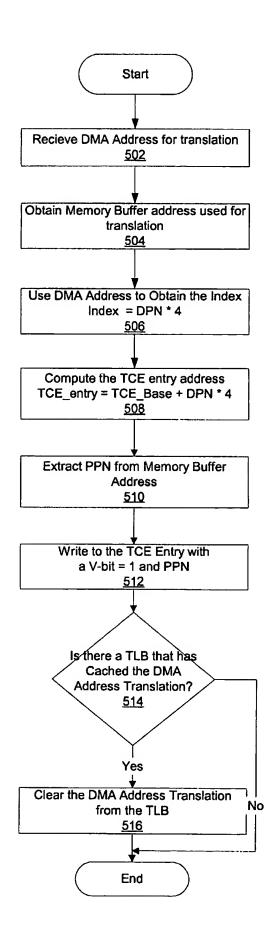
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Figure 3 32bit DMA Address AUS920040058US1 Method to Allow PCI Host Brige (PHB) to Handle Pre-Fetch Read Transactions on the PCI Bus which Access System Memory Through Translation Control Entry (TCE) Table 19 20 31 Page 3 of 6 DPN Offset 0 <u>306</u> 308 .326 Reserve page 310 309 10 11 RPN **↓**29 30 31 1 1 RPN DPN 315 00 <u>317</u> 000000000 0 <u>311</u> 312 318 RPN 1 RPN RPN 322 TCE Table Base Register TCE BASE **Physical Memory Address** <u>320</u> 0 23 24 39 PPN Offset

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